REMARKS

This response is submitted in reply to the Official Action dated November 6, 2002 ("the Action"). In the Action, the Examiner required a restriction for:

Group I.	Claims 29-61, drawn to a semiconductor device, classified in class 257, subclass 762;
Group II.	Claims 1-28 and 62-68, drawn to a method of making a semiconductor device, classified in class 438, subclass 687.

Applicant hereby elects, without traverse, Claims 1-28 and 62-68 and newly added Claims 69-76 of Group II drawn to methods of making semiconductor devices. Claims 29-61 have been canceled without prejudice to Applicant's right to pursue these claims in a divisional application. In addition, Applicant agrees that unpatentability of claims of Group I would not necessarily imply unpatentability of claims of Group II.

In addition, Applicant notes that the Office Action refers to: "performing the steps in the order of providing a first passivation layer on a first barrier layer; providing a solder structure on the first passivation layer and then selectively providing a second passivation layer on a second barrier layer" (Office Action, page 2) as an example that devices of Group 1 could be made by processes different from those of Group II. The Applicant respectfully submits, however, that the order cited in the Office Action is not recited in the independent claims of Group II.

Applicant respectfully submits that this application is now in condition for substantive examination, which action is requested. If any extension of time for the accompanying response or submission is required, Applicant requests that this be considered a petition therefor. The Commissioner is hereby authorized to charge any additional fee, which may be required, or credit any refund, to our Deposit Account No. 50-0220.

Respectfully submitted,

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Date of Signature: December 4, 2002

Version With Markings To Show Changes Made

In The Title:

Please enter the amendment of the title at all occurrences thereof to recite:

METHODS OF FORMING METALLURGY STRUCTURES FOR WIRE AND SOLDER BONDING ~~{AND RELATED STRUCTURES}~~

In The Claims:

Please enter the cancellation of Claims 29-61.

Please enter new Claims 69-76.

69.(New) A method of forming an electronic device comprising:

forming an input/output pad on a substrate;

forming a bonding structure on the input/output pad, the bonding structure including a barrier layer comprising nickel on the input/output pad, and a solder structure on the barrier layer.

70.(New) A method according to Claim 69 further comprising:

forming an under bump metallurgy layer between the nickel barrier layer and the input/output pad.

71.(New) A method according to Claim 70 wherein the under bump metallurgy layer comprises an adhesion layer on the input/output pad, and a conduction layer on the adhesion layer.

72.(New) A method according to Claim 71 wherein the adhesion layer comprises a titanium layer, and wherein the conduction layer comprises a copper layer.

73.(New) A method according to Claim 69 wherein the barrier layer comprises a nickel layer free of lead and an alloy layer including nickel and lead between the nickel layer free of lead and the solder structure.

74.(New) A method according to Claim 69 further comprising:

forming a second input/output pad on the substrate;

forming a second bonding structure on the second input/output pad, the second bonding structure including, a second barrier layer comprising nickel on the second input/output pad, and a gold layer on the barrier layer comprising nickel; and

bonding a wire to the second bonding structure.

75.(New) A method according to Claim 69 further compising:

bonding a second substrate to the solder structure.

76.(New) A method according to Claim 69 further comprising:

forming a protective insulating layer on the substrate and on portions of the input/output pad so that portions of the input/output pad are exposed through the protective insulating layer.